

DEVELOPMENT OF LOW COEFFICIENT OF THERMAL EXPANSION
COMPOSITE SUBSTRATE FOR ELECTRONIC PACKAGING USING FINITE
ELEMENT METHOD

PANG HOOI SAN

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Dedicated to,
My beloved parents, family and friends.

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ABSTRACT

Coefficient of thermal expansion (CTE) mismatch between the different material layers in the substrate leads to residual warpage and stresses. Such deformation adds additional mechanical constraints to solder joint attached on the surface of substrate and subsequently leads to solder joint reliability issue of the electronic package. Thus, a new composite material was evaluated with the aim to reduce both in-plane and out-of-plane CTE of the core substrate. In this study, equivalent thermo-mechanical and viscoelastic properties of silica-filled epoxy were predicted with finite element method. The silica-filled epoxy was served as the matrix of the core substrate and woven glass were embedded as few layers in the matrix phase. Viscoelastic response of the matrix phase and resulting orthotropic of the multilayered substrate were modeled. Substrate warps in concave shape after subjected to curing temperature due to CTE mismatch and asymmetry of geometry. For surface mount assembly, accumulated inelastic strain in the critical solder joint with low CTE composite substrate is lower than that of with conventional FR-4 substrate during the solder reflow and temperature cycles. In addition, the predicted life cycle of the low CTE composite assembly is 36.9 % longer compared to assembly with FR-4 substrate.

ABSTRAK

Ketidakseimbangan Pekali Pengembangan Haba (CTE) antara pelbagai jenis lapisan bahan telah menyebabkan pembentukan lenturan dan tegasan baki. Perubahan bentuk ini telah menambahkan lagi sekatan mekanikal yang berlebihan kepada sambungan pateri yang terikat pada permukaan substrat selanjutnya membawa masalah keboleharapan sambungan pateri kepada pakej elektronik. Oleh sebab itu, bahan komposit yang baru telah dikaji dengan tujuan mengurangkan CTE bahan sama ada dalam satah melintang atau satah mendatar. Dalam kajian ini, sifat kesamaan terma-mekanikal dan viskoelastik bagi epoksi yang dicampur dengan silika telah dijangka dengan menggunakan kaedah unsur terhingga. Epoksi yang dicampur dengan silika merupakan matrik bagi teras substrat dan beberapa lapisan tenunan kaca telah dipacakkan ke dalam silika-epoksi. Matrik yang bersifat viskoelastik dan substrat pelbagai lapisan yang bersifat ortotropik telah dihasilkan. Substrat melentur dengan bentuk cekung selepas melalui suhu pengerasan disebabkan ketidakseimbangan CTE dan geometri yang tidak simetri. Bagi penyambungan pajangan permukaan, nilai terikan tidak elastik yang berkumpul di sambungan pateri kritikal dalam komposit substrat yang CTE rendah adalah lebih rendah jika dibandingkan dengan substrat FR-4 semasa *reflow* pateri dan kitaran haba. Tambahan pula, jangkaan hayat kitaran bagi penyambungan yang mempunyai komposit yang CTEnya rendah adalah 36.9% lebih panjang berbanding dengan penyambungan dengan substrat FR-4.

TABLE OF CONTENTS

CHAPTER	TITLE	PAGE
	TITLE PAGE	i
	DECLARATION PAGE	ii
	DEDICATION PAGE	iii
	ACKNOWLEDGEMENT	iv
	ABSTRACT	v
	ABSTRAK	vi
	TABLE OF CONTENTS	vii
	LIST OF TABLES	xi
	LIST OF FIGURES	xii
	LIST OF SYMBOLS	xvi
	LIST OF APPENDIXES	xvii
 CHAPTER 1	 INTRODUCTION	 1
	1.1 Background	1
	1.2 Objectives	5
	1.3 Scope of Study	5
	1.4 Significance of Study	6
	1.5 Thesis Layout	7

CHAPTER 2	LITERATURE REVIEW	8
2.1	Electronic Packaging	8
2.2	Substrate Material	10
2.3	Substrate Fabrication	13
	2.3.1 Conductor Patterning	14
	2.3.2 Multilayer Substrate Lamination	15
	2.3.3 Hole and Via Formation	15
	2.3.4 Solder Mask	16
2.4	Development of the Substrate Material	16
	2.4.1 Low CTE Substrate Material	19
	2.4.2 Effect of Silica and Woven Glass to the CTE of Epoxy	21
2.5	Warpage Studies	25
	2.5.1 Warpage and Solder Joint Reliability	25
	2.5.2 Warpage and Viscoelastic Behavior	27
2.6	Viscoelastic	28
	2.6.1 Definition	28
	2.6.2 The Maxwell and Voigt Model	29
	2.6.3 Temperature Dependent Behavior	32
	2.6.4 Time Temperature Superposition and Master Curve	33
2.7	Viscoplastic Behavior	35
	2.7.1 Classical Model	35
	2.7.2 Unified Inelastic Strain Model	36
 CHAPTER 3	 METHODOLOGY- MODELING APPROACH	 39
3.1	Modeling Approach	39
3.2	Modeling Assumptions	41
3.3	Finite Element Modeling	41
	3.3.1 Stage I – SiO ₂ /Epoxy Composite	41
	3.3.2 Stage II – Substrate with Composite Core	44

3.3.2.1 Geometry of the Substrate Layers	44
3.3.2.2 Material Properties	46
3.3.2.3 Boundary Conditions	47
3.3.2.4 Curing Temperature Profile	48
3.3.3 Stage III - Surface Mount Assembly Model	49
3.3.3.1 Geometry and Dimensions	49
3.3.3.2 Material Properties	50
3.3.3.3 Boundary Condition and Meshing	52
3.3.3.4 Reflow and Temperature Cycles	54
3.4 Viscoelastic Constitutive Model	55
 CHAPTER 4 RESULTS AND DISCUSSIONS -COMPOSITE MODEL	 58
4.1 Woven Glass Fiber Reinforced Epoxy Matrix Composite	58
4.2 Silica-Filled Epoxy Composites	61
4.3 Silica-Filled Epoxy Reinforced With Woven Glass	65
 CHAPTER 5 RESULTS AND DISCUSSIONS - SUBSTRATE MODEL	 69
5.1 Warpage Condition	69
5.2 Evolution of von Mises Stress	70
5.3 Shear Stress Distribution	74
 CHAPTER 6 RESULTS AND DISSCUSSIONS - SURFACE MOUNT ASSEMBLY	 75
6.1 Solder reflow Process	75
6.2 Temperature Cycles	79
6.3 Stress Strain Hysteresis Loops	80

CHAPTER 7	CONCLUSIONS AND SUGGESTIONS	82
7.1	Conclusions	82
7.2	Suggestions and Recommendations	84
	REFERENCES	85
	APPENDICES	92

LIST OF TABLES

TABLE NO.	TITLE	PAGE
2.1	Properties of the base materials used for chip packages (Roadmap of Packages Technology: Substrate Materials for LSI Packages)	17
2.2	Properties of the base materials used for PCBs (Roadmap of Packages Technology: Substrate Materials for Printed Wiring Board)	17
2.3	Summary of low CTE substrate materials	20
3.1	Material properties of woven glass and silica filler	42
3.2	Temperature dependent properties used in the substrate model	46
3.3	Properties of material used in surface mount assembly model	51
3.4	Properties of FR-4 composite	51
3.5	Data of horizontal shift factor, $\log a_T$ for molding compound	56
4.1	Equivalent orthotropic material properties of epoxy with 30% woven glass and 20% silica	67
6.1	Results summary after the solder reflow process	76
6.2	The predicted life of solder joint for the FR-4 and composite substrate	81

LIST OF FIGURES

FIGURE NO.	TITLE	PAGE
1.1	Schematic draw of a typical packaging hierarchy. (Harper, 2000)	2
1.2	A schematic draw of a flip chip package	3
2.1	SEM image of wire bonding at the chip area	9
2.2	SEM image of solder bumps on chip	9
2.3	Schematic diagram of substrate structure	11
2.4	Copper pattern of a multichip package (Moore and Jarvis, 2002)	12
2.5	Schematic diagram for x, y, z-axis direction	16
2.6	CTE of epoxy with different weight percentage of silica filler at 25 °C.	22
2.7	Young Modulus, E versus CTE of silica-filled epoxy compared to substrate material, polyimide, BT and FR-4. Reference temperature is 25°C	22
2.8	The effects of silica filler content to the CTE and elastic modulus of silica-filled epoxy (Harper, 2004).	23
2.9	CTE of FR-4 with various resin/glass ratio (Wu <i>et al</i> , 1996).	24
3.1	Schematic diagram of the modeling approach	40
3.2	Finite element models of SiO ₂ filled epoxy	41
3.3	SiO ₂ filled-epoxy model with boundary condition and force applied	42
3.4	Temperature dependent Young modulus, E and Secant	43

	CTE of epoxy resin (Adolf <i>et al.</i> , 2004)	
3.5	Master curve of shear relaxation modulus versus reduce time of epoxy resin (Adolf <i>et al.</i> , 2004)	43
3.6	Exploded view and dimensions of the quarter multilayer substrate	45
3.7	Boundary condition of substrate model data	47
3.8	Curing temperature profile of substrate model	48
3.9	Exploded view and dimensions of the BGA test package and solder joint	49
3.10	Boundary condition of surface mount assembly model	52
3.11	Finite element meshing of the test assembly and critical solder joint	53
3.12	Reflow and thermal cycle temperature profile	54
3.13	DMA Experimental data of storage modulus, G' versus frequency, ω with constant temperature from 68.87°C to 219.66°C of molding compound electronic packages. (Yeung, 1997).	55
3.14	Master curve of storage modulus $\log G'$ versus reduced time $\log t/a_T$ of molding compound	57
4.1	Comparison of in-plane material properties between the simulation woven-glass reinforced epoxy and the FR-4. (Reference Temperature = 25°C)	59
4.2	Simulation results of in-plane and out-of-plane CTE of epoxy resin after adding with different volume percentage of woven glass. (Reference temperature = 25°C and 150°C accordingly)	60
4.3	Comparison of temperature dependent Young modulus, E and secant CTE of silica-filled epoxy and epoxy	61
4.4	Comparison between master curves generated using data from finite element (points) and experiment (line)	62
4.5	Shear relaxation modulus versus time for the silica-filled epoxy at different temperatures with applied of strain	63

	0.1%	
4.6	Comparison of shear relaxation modulus versus reduced time for silica-filled epoxy and epoxy	64
4.7	FEM Stress relaxation of silica-filled epoxy and pure epoxy. Temperature, 65°C with constant strain 0.1%.	65
4.8	Simulation results of in-plane and out-of-plane CTE of 30%v/v woven glass composite after adding with different volume percentage of silica filler. (Reference temperature = 25°C and 150°C accordingly)	66
4.9	Comparison of the temperature dependent secant CTE of low CTE composite and FR-4	68
4.10	Comparison of the temperature dependent Young Modulus of low CTE composite and FR-4.	68
5.1	(a) Contour plot of warpage condition after curing process. (b) Magnitude of vertical displacement from center to the edge of the substrate.	70
5.2	Evolution of von Mises stress for elastic and viscoelastic core substrate at the edge of core substrate during curing process	72
5.3	Comparison of von Mises stress evolution curves between elastic FR-4 and viscoelastic SiO ₂ -filled epoxy cores during heating process	73
5.4	Contour plot of shear stress between the interface of the core substrate and copper layer	74
6.1	(a) Contour plot of the warpage condition of the test package after reflow process. (b) The distribution of the accumulated inelastic strain in the critical solder	76
6.2	The side view of the warpage assembly and the deformation condition of the critical solder joint.	77
6.3	Evolution of accumulated creep strain in the critical solder for FR-4 and composite substrate during reflow process	78

6.4	Evolution of von Mises stress in the critical solder joint for assembly by using FR-4 substrate and composite core substrate during reflow process	78
6.5	Comparison of the evolution of inelastic strain in critical solder for assembly by using FR-4 and low CTE substrate during the temperature cycles	79
6.6	Stabilized hysteresis loops (six cartesian components) of at the critical element of the solder joint	80
6.7	Schematic draw of the deformation of solder joints after the thermal cycle.	81

LIST OF SYMBOLS

ASIC	-	Application-specific IC
BGA	-	Ball grid array
BT	-	Bismaleimide triazine
C_1, C_2	-	Material constant
C4	-	Controlled collapse chip connection
CBGA	-	Ceramic ball grid array
CE	-	Cyanate ester
COPNA	-	Polycondensed fused polynuclear
CSP	-	Chip scale package
CTE	-	Coefficient of thermal expansion
DCA	-	Direct chip attach
DMA	-	Dynamic Mechanical Analysis
E	-	Young's modulus
FEM	-	Finite element method
FCOB	-	Flip chip on board
FR-4	-	Fire Retardant Epoxy
G	-	Shear modulus
G'	-	Storage shear modulus
G_0	-	Instantaneous shear modulus
IC	-	Integrated circuit
I/O	-	Input/Output
$\log a_T$	-	Horizontal shift factor
MBGA	-	Metal ball grid array
N_f	-	Number of cycles to failure
PCB	-	Printed circuit board

PBGA	-	Plastic ball grid array
PTH	-	Plated through hole
Q	-	Activation energy
R	-	Gas constant
SEM	-	Scanning electronic microscopic
SiO ₂	-	Silica
t	-	Reduced time
T, Temp	-	Temperature
T _g	-	Glass transition temperature
TSOP	-	Thin small outline package
TTS	-	Time-temperature superposition
U2	-	Vertical displacement
UV	-	Ultra violet
w	-	Frequency
ε	-	Strain
ε_{in}	-	Inelastic strain
$\varepsilon_p, \Delta\gamma$	-	Plastic strain range
σ	-	Stress
σ_{vm}	-	Von mises stress
τ	-	Relaxation time
ν	-	Poisson's ratio
γ	-	Shear strain
η	-	Viscosity

LIST OF APPENDICE

APPENDIX	TITLE	PAGE
A	Paper of Conference on Manufacturing and Electronic Technology (COMET). January 14-15, 2006. Skudai, Malaysia: UTM-SME	92

CHAPTER 1

INTRODUCTION

This study evaluates a candidate polymer matrix composite as a potential material for use as substrate in an electronic package. Emphasis is placed on the potentially low coefficient of thermal expansion (CTE) of the composite. Usage of such low CTE material could considerably reduce substrate warpage, thus contribute to improved reliability of the package. This chapter presents the background, objectives, scope and significance of the research. Layout of the thesis is also included in this chapter.

1.1 Background

Packaging technology is one of the fast growing areas in industries where its development is accelerating towards smaller, lighter, faster and low cost products. This advancement gives a big challenge to electronic packaging industry because rapid development of the silicon chip requires a comparable but smaller package so as to meet the demand for multi-functional, as well as small and lighter electronic products. This high-density component experiences temperature excursions during fabrication and operation of the package. Hence, the concern of thermal mismatch becomes more

stringent. Different CTE values not only lead to warpage and residual stress in the package but also contribute to package cracking and delamination problems.

Typical packaging hierarchy (Figure 1.1) illustrates the different levels of packaging. The zero level packaging includes integrated circuit (IC) chip fabrication. An IC chip is a collection of components connected to form a complete electronic circuit that is manufactured on a single piece of semiconductor material. The first level packaging is the assembly of chip and substrate to form a single or a multiple chip module. The second level packaging is the assembly of chip module and other component on PCBs. The third level packaging involves several PCBs plugged into a motherboard.

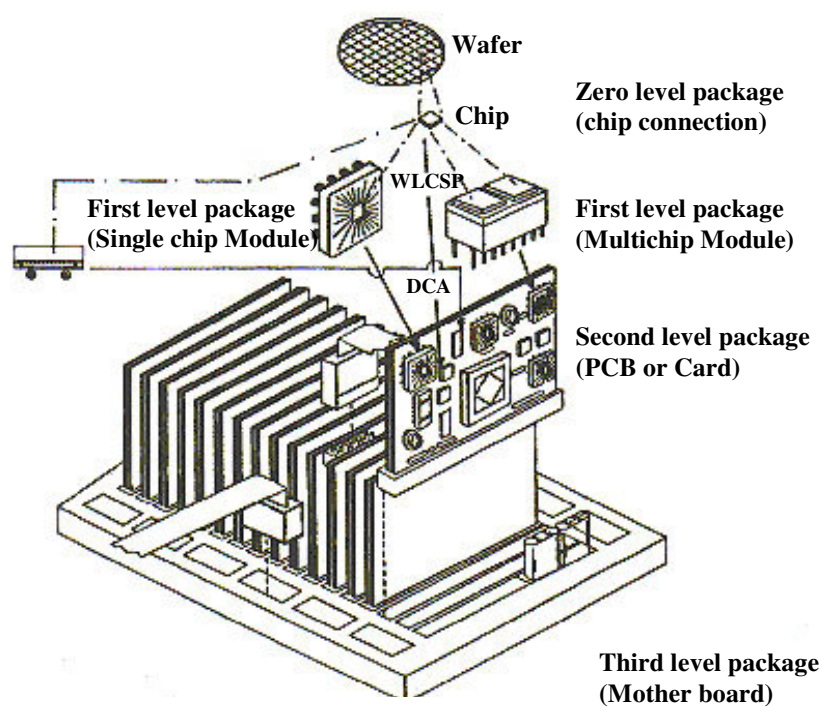


Figure 1.1 Schematic draw of a typical packaging hierarchy. (Datta, 2005)

The main function of an IC package is to be the electrical connections between the IC chip and board. It gives the mechanical support and protection from the environmental and chemical agents. Besides, it is also designed to allow heat transfer from the chip.

The chip level-interconnection technologies currently used in the semiconductor industry include wire bonding and flip chip solder connection. Wire bonded electrical connections are created at assembly stage by attaching a fine wire around the perimeter of the chip. Meanwhile, flip chip interconnection is an area array configuration in which the entire surface of the chip can be covered with solder bumps for the highest possible input/output (I/O) counts.

Flip chip technology was first introduced by IBM in 1960s and the joining process was named controlled collapse chip connection (C4) technology (Totta, 1969). A typical flip chip consists of silicon chip, solder joint, underfill and substrate as shown in figure 1.2. The chip is attached on the substrate with solder interconnections. Underfill is applied to minimize the thermal mismatch deformation in the solder joints.

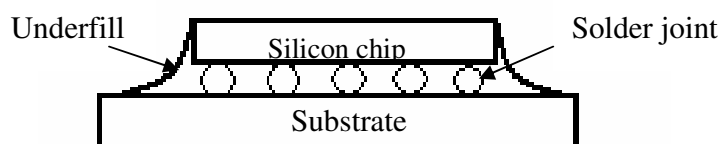


Figure 1.2 A schematic draw of a flip chip package.

A typical flip chip package consists of a stack of materials with vastly different CTEs. Heat is generated during operation of the package. The large difference in CTE values between silicon die (2 ppm/°C) and organic substrate (16 ppm/°C) causes the package to warp. High temperature gradient and CTE mismatch also induces thermal strain and stress in solder joints.

Multilayered substrate in the flip chip package is made of different types of material layers such as solder resists, dielectrics, core substrate, copper traces and plated through holes. When these layers are bonded together during fabrication through pressure and heating process, different expansion rates among these layers result in the residual warpage to form either a concave or a convex shape. Such deformation adds additional mechanical constraints to solder joint attached on the surfaces.

Since warpage is primarily governed by stiffness of the core substrate, potential low CTE composite core is proposed. In this study, a new composite material is evaluated to be employed as a core of the layered substrate. The epoxy matrix was mixed with silica filler to reduce the out-of plane thermal expansion while the in-plane expansion is primarily governed by woven glass. The silica-filled epoxy reinforced with woven glass composite is expected to lower the CTE in both in-plane and out-of plane directions. The performance of the new substrate with composite core is examined in comparison to the traditional FR-4 substrate plates.

1.2 Objectives

The objectives of the study are:

1. To develop and to evaluate a low CTE (and high modulus) composites with epoxy matrix and silica powder and woven glass fibers.
2. To establish the equivalent viscoelastic and thermo-mechanical properties of the silica-filled epoxy composite.
3. To simulate deformation response of a multilayer substrate with a low CTE composite core during the curing process.
4. To study the solder joint reliability of the surface mount assembly using the newly developed low CTE composite.

1.3 Scopes of Study

The scope of this study covers the following:

1. Examination of composite core:
 - To establish the material properties and viscoelastic behaviour of silica-filled epoxy composite using the properties of constituents.
 - To establish the properties of glass-fibre reinforced silica-filled epoxy composite.
2. Finite element modeling of multilayered substrate with composite core during typical curing temperature cycle.
3. Finite element modeling of surface mount assembly with different substrate materials:
 - To evaluate the current FR-4 substrate (reference case)
 - To evaluate substrate with low CTE composite core

The parameters for viscoelastic constitutive model of the epoxy are extracted from results of experimental test published in literature. Although glass transition temperature - T_g is relatively low for current application in an electronic package, the procedure illustrated in this study is identical if other polymer is considered, provided with sufficient data is available.

1.4 Significance of Study

The viscoelastic (time-dependent) response of the substrate is established in this study. This viscoelastic material model contributes to greater accuracy when employed in finite element modeling of electronic packages for reliability prediction. In addition, the methodology can be adopted for other core material of substrate with available experimental data.

Different percentage of silica filler and woven glass reinforcement produce composite with various CTE and elastic modulus properties. Parametric study can be performed to optimise warpage of substrate, thus improve reliability of solder joints in the surface mount assembly and subsequently affect the thermal fatigue life of the test assembly.

1.5 Thesis Layout

There are seven chapters in the thesis. Chapter one introduces the background of the research and adequately describes the problem arise. The scopes, objectives and significance of study are also included in this chapter.

Chapter two reviews the literature studies on the related topics. It includes an overview of electronic packaging, substrate material and its fabrication process. Besides, works related to the low CTE base material and warpage constitutive model are critically reviewed. The behaviour of viscoelastic and unified inelastic are presented.

Chapter three explains about the modeling approach and assumptions. The details of the geometry, material properties, boundary conditions and temperature loading of each model are presented. At the last section, example of viscoelastic constitutive model is provided.

Chapter four gives the results of composite model in term of elastic modulus and coefficient of thermal expansion. Different percentages of silica and woven glass were added in the epoxy matrix. The equivalent properties of silica-filled epoxy are illustrated in graphs.

Chapter five discusses about the warpage condition and evolution of von Mises stress of the substrate. Shear stress distribution of core substrate is also included.

Chapter six presents the warpage condition of the test assembly package. The evolution of von Mises stress and inelastic strain in critical solder joint with the used of low CTE composite substrate during reflow and thermal cycle are compared with that of the FR-4 substrate.

Finally, the conclusions of this work are given in Chapter 7 along with the recommendations for the future works.